14, 18, 20, 21, 23, 25, 28, 30, 31, 33, 35 and 36 are amended and new claims 38-46 are added to recite subject matter to which Applicant is already entitled. Applicant respectfully submits that no issue of new matter is presented by this Amendment. Accordingly, claims 1-8 and 11-46 are now pending in the subject application, and for at least the reasons solicited hereinbelow, are in condition for allowance.

Please note that the Office Action Summary (PTO-326) indicates that claims 1-8 and 12-37 are pending in the subject application, while page 2 of the Office Action indicates that claims 1-8 and 11-37 are currently pending. Since claim 11 has not been canceled during the prosecution of the subject application, Applicant contends that claims 1-8 and 11-37 are pending herein. In this regard, claim 11 is not subject to a prior art rejection, and thus, which Applicant assumes is the result of this oversight.

Initially, the Office Action rejects claims 1-8, 12-22 and 28-31 under 35 U.S.C. §112, first paragraph as containing inadequate support in the specification for the claim recitation directed to an insulating film comprising resinous material being used as a leveling surface. By the above Amendment, claims 1, 11, 12, 18 and 28 are amended to overcome the above-noted rejection. In particular, claims 1, 11, 12, 18 and 28 are amended to delete the recitation "said interlayer insulating layer having a leveling surface". Accordingly, reconsideration and withdrawal of the amendment is respectfully solicited.

The Office Action rejects claims 1-8 and 12-37 under the judicially created doctrine of double patenting over claims 1-68 of U.S. Patent No. 6,242,758. In order to obviate the above-noted rejection and pursuant to 37 C.F.R. §1.321, Applicant files concurrently herewith a *Terminal Disclaimer* that disclaims the statutory term of any patent that may be granted on the above-referenced application extending beyond the expiration date of the full statutory term as defined by 35 U.S.C. §§154-156 and 173 of

U.S. Patent No. 6,242,758.

Accordingly, Applicant respectively submits that the pending claims are in proper condition for allowance and consideration and withdrawal of the pending rejections are requested. If the Examiner believes further discussions with Applicant's representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

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MARKED UP VERSION OF AMENDED CLAIMS

1. (Three Times Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, [said interlayer insulating layer having a leveling surface,]

[wherein] said thin film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

2. (Amended) The device of claim 1 wherein said [semiconductor layer constitutes] thin film transistor is an inverted-staggered thin-film transistor.

3. (Amended) The device of claim 1 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

5. (Twice Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

[wherein] said thin film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, [and]

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

6. (Amended) The device of claim 5 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

11. (Three Times Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; [and]

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, [said interlayer insulating layer having a leveling surface,]

[wherein] said thin film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

12. (Three Times Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, [said interlayer insulating layer having a leveling surface,]

[wherein] said thin film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate

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insulating film therebetween,

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

13. (Amended) The device of claim 11 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

14. (Amended) The device of claim 12 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

18. (Three Times Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising resinous material provided over said thin film transistor, [said interlayer insulating layer having a leveling surface,]

[wherein] said thin film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

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a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said channel formation region comprises amorphous silicon.

20. (Amended) The device of claim 18 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

21. (Amended) The device of claim 18 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

23. (Three Times Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor;

at least one pixel electrode provided on said interlayer insulating layer,

[wherein] said thin film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate

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insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

25. (Amended) The device of claim 23 wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

28. (Three Times Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising resinous material provided over said thin film transistor, [said interlayer insulating layer having a leveling surface,]

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said channel formation region comprises microcrystalline silicon.

30. (Amended) The device of claim 28 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

31. (Amended) The device of claim 28 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

33. (Three Times Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

[wherein] said thin-film transistor [comprises] comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, [and]

wherein said semiconductor layer comprises microcrystalline silicon.

35. (Amended) The device of claim 33 wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

36. (Amended) The device of claim 33 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of

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acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

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